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United International Journal of Engineering and Sciences (UIJES)
An International Peer-Reviewed (Refereed) Engineering and Science Journal Impact Factor:7.984(SJIF)
Volume-4, Special Issue-3; ISSN: :2582-5887

A Novel 1-Ø Asymmetric Multi-Cell Cascaded Multilevel Inverter for Photovoltaic Arrays

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DOI:10.53414/UIJES:2024.43.259

***Abstract* – The distributed renewable energy source (DRES) such as photovoltaic arrays established single-phase inverter is typically advocated in the micro grid system. A short while ago, a number of multilevel inverters designs became available. The most common structure created from such designs is a cascaded multilevel inverter. Using conventional low voltage component designs, this kind of multilevel inverter incorporates a medium voltage output on the basis of a series connection of power cells. This odd confess one may use several topologies to generate good quality output waveforms for voltage and current. This paper's goal is to get a greater output voltage level while using fewer switches, spending less money, and achieving lower THD values. Asymmetric multi-cell CMLI topology is used to carry it out. Thus, a proposed 85 level asymmetric multi-cell cascade multilevel inverter is introduced in this article. When compared to other CMLI topologies, this one is the best in enhancing the fundamental component and lowering the THD value while utilizing fewer switches. The grid-connected, 85-level asymmetrical CMLI receives the DRES as photovoltaic input. MATLAB/SIMULINK software is used to verify the proposed topology, and the results are shown.**

***Keywords* – Cascaded H-Bridge MLI, Multi-Cell CMLI, Total Harmonic Distortion (THD).**

I. INTRODUCTION

The public's ongoing concern over climate change and global warming has led to major efforts toward the development of environmentally friendly DRES or renewable energy resources. These days, it's essential to integrate interface converters of DRES, such as solar, fuel cells, micro turbines, and wind power, into the micro grid system in addition provide premium electric power that is reliable, efficient, and has high power quality[1-2]. In these kinds of systems, the majority of distributed renewable energy sources typically provide a DC voltage that fluctuates widely based on different load scenarios. As a result, a DC-AC power processing interface that complies with utility grid standards, residential and commercial shopping mall requirements, and industry standards is required. [3-5].

Different type of converter topologies have been designed for distributed renewable energy resources [6-9] that exhibit efficient power flow control appearance whether in Stand-alone or grid-connected operation. Among them, solutions that make use of high-frequency transformers or make no performance of Transformers at all have been investigating to decrease size, weight and expense. To maintain international standards allow the use of grid-connected power converters without galvanic isolation, thus allowing called " transformerless" architectures for low rating medium power applications.

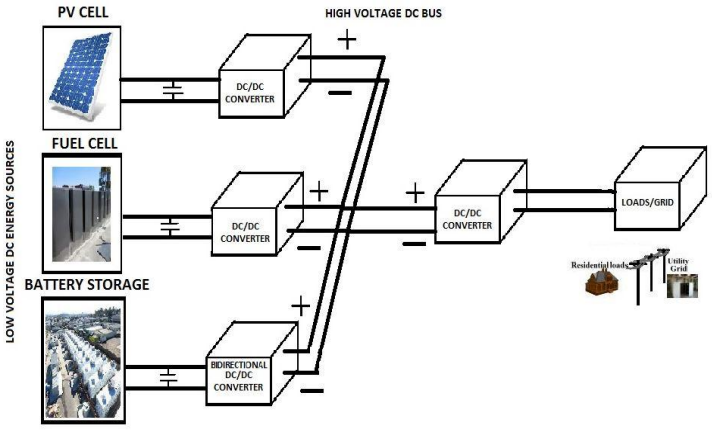

Fig.1 Configuration of Multi cell-CMLI for various DRES

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The figure shows above DES are connected to loads/grid through DC-DC converter and DC-AC Inverter. Inverter is an electrical power converter which conversion from fixed DC to AC voltage. The inverter doesn't create a pure sinusoidal wave as an infinite number of odd harmonics here in it. When the two level wave is applied for the electrical gadgets it dwindle the life span of electrical working gadgets. This problem is resolve by with multilevel inverters (MLI) in which bring into being stepped voltage wave shape which is equivalent to sinusoidal wave form [10-11].

The sources of input can be taken as Photovoltaic Cells, fuel cells etc. The most widely recognized semiconductor switching devices are MOSFET, IGBT. A typical power inverter circuit of device should a moderately stable DC power source capable of supplying enough current for the deliberate power demands of the system. The input voltage depends up on the design and power of the inverter.

MLIs having three types, they are namely as Diode clamped MLI, Flying capacitor MLI and Cascaded H-bridge multilevel inverters (CHBMLI). Along with all topologies, CHBMLI achieve the higher output voltage and power levels and higher reliability due to its standard topology. Again CHBMLI can be classified into two types which are symmetrical and asymmetrical CHBMLI [12-13]. Among that symmetrical CHBMLI means the input DC sources of the CHBMLI are equal in voltage magnitude. Whereas Asymmetric CHBMLI means the input DC sources are not equal in the voltage value. The proposed system of Asymmetric multi-cell CMLI has to generate 25 level, 65 level and 85 level output voltage. In this paper 65 level and 85 level output voltage and compare the THD value of both presented. The input sources can be taken as photovoltaic cell for proposed system of 85 level asymmetric multi-cell CMLI connected to grid.

II. PHOTO VOLTAIC SYSTEM

A photovoltaic system directly converts sunlight into electricity. The basic device of a PV system is the PV cell. Cells may be grouped to from panels or arrays. The voltage and current available at the terminals of PV device may directly feed small loads such as lighting systems and DC motors. A photovoltaic cell is basically a semiconductor diode whose p-n junction is exposed to light. Photovoltaic cells are made of several types of semiconductors using different manufacturing processes. The incidence of light on the cell generates charge carriers that originate an electric current if the cell is short-circuited.

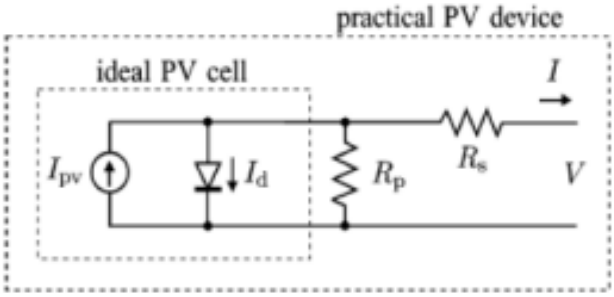

Fig. 2 Equivalent circuit of a PV device including the series and parallel resistance

The equivalent circuit of PV cell is shown in Figure 2. In the above diagram the PV cell is represented by a current source in parallel with diode. R_s and R_p represent series and parallel resistance respectively. The output current and voltage from PV cell are represent by I and V.

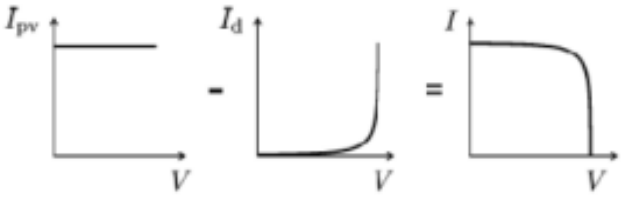

Fig. 3 Characteristic I-V curve of the PV cell

The I-V characteristics of PV cell is shown in the above Figure 3. The net cell current I is composed of the light-generated current I_{PV} and diode current I_d.

$$I = I_{pv} - I_d \qquad (1)$$

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Where

$I_d = I_0 \exp\left({}^{qV}/_{akT}\right)$

Io = leakage current of the diode

q = electron charge

k = Boltzman constant

T = temperature of pn junction

a = diode ideality constant.

The basic equation (1) of a PV cell does not represent the I-V characteristic of practical PV array. Practical array are composed of several connected PV cells and the observation of the characteristics at the terminals of the PV array requires the inclusion of additional parameters to the basic equation.

$$I = I_{pv} - \left[\exp\left(V + \frac{R_s I}{V_t a}\right) - 1\right] - \frac{V + R_s I}{R_p} \qquad (2)$$

Where

$V_t = N_s kT/qs$ is the thermal voltage of the array with N_s cells connected in series. Cells connected in parallel increase the current and cells connected in series provide greater output voltages. Th I-V characteristics of a practical PV cell with maximum power point (MPP), short circuit current (Isc) and open circuit voltage (Voc) is shown in Figure 4. The MPP represents the point at which maximum power is obtained.

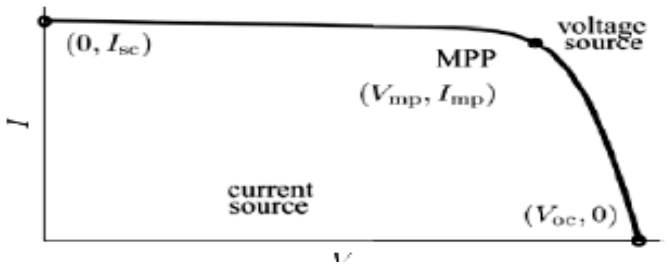

Fig. 4 I–V The practical PV cell Characteristics

Vmp and Imp are voltage and current at MPP respectively. The output from PV cell is not the same throughout the day, it varies with varying temperature and insolation (amount of radiation). Hence with varying temperature and insolation maximum power should be tracked so as to an achieve the efficient operation of PV system.

III. PROPOSED SYSTEM

In this proposed system, 25 level multi-cell CMLI is presented. In this topology, high quality output voltage and current waveforms are achieved with less number of switches. For example, to obtain 25 levels in this topology only 12 switches are essential. In this multi-cell topology, multiple numbers of non-isolated DC voltage sources are given to the input. Other than the full bridge (4 switches) extra switching components are given to power cells as series and parallel connection. By this topology, switching losses are reduced, cost is effective, lower voltage rating devices can be used, leading to reduction in Electro Magnetic Interference and voltage stress (dv/dt) is dwindled. Mainly this topology is used for low voltage high power applications. The proposed 25 level asymmetric multi-cell CMLI block diagram is as shown in the Fig.5.

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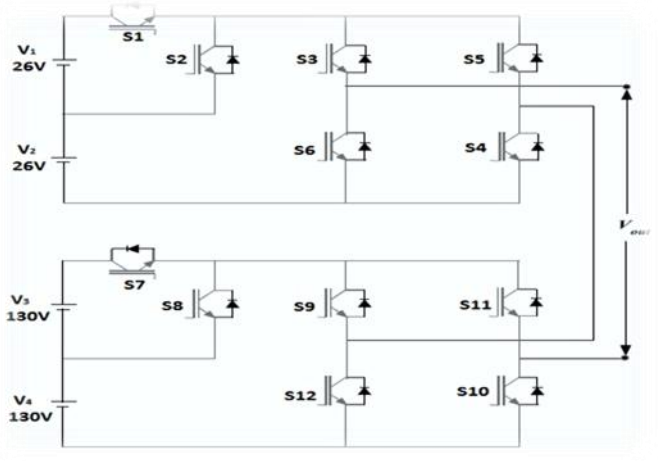

Fig. 5 Proposed 25 level asymmetric multi-cell CMLI

The above Fig.5 Shows Proposed 25 level asymmetric multi-cell CMLI having 12 switches and 4 DC sources but compared to Cascaded H-bridge MLI having 48 switches and 12 DC sources. In this system, the input supply to the system is 26V, 26V, 130V, 130V. There are a total of 312 volts. There are total of two bridge circuits, each bridge has two inputs and the first bridge circuit consists of inputs as 26V and 26V, whereas second bridge circuit of 130V and 130V correspondingly. The first arm of the first bridge is considered as the positive load terminal. The second arm from the first bridge is connected to the first arm of the second bridge circuit. The second arm of the second bridge circuit is the negative load terminal.

The proposed system is operating in 25 modes and these are controlled by changing the switching periods of the switching devices (IGBT). The table I showing the intervals of the switching at different levels of voltages is shown in table I. The different modes operation is represented as following.

The same proposed system of asymmetrical CMLI to generate 65level and 85 level output voltage by cascaded of one additional bridge (6 switches and 2 DC sources).

Table I: Switching Table for Proposed System

Voltage	Switches
0V	S1, S3, S5, S7
26V	S1, S2, S5, S7, S10
52V	S1, S2, S5, S7, S9
78V	S3, S4, S5, S6, S9, S12
104V	S3, S4, S5, S6, S10, S12
130V	S1, S3, S5, S6, S12
156V	S1, S2, S5, S6, S10, S12
182V	S1, S2, S5, S6, S9, S12
208V	S3, S4, S5, S6, S9, S11
234V	S3, S4, S5, S6, S10, S11
260V	S1, S3, S5, S6, S11
286V	S1, S2, S5, S6, S10, S11
312V	S1, S2, S5, S6, S9, S11
-26V	S3, S4, S5, S7, S10
-52V	S3, S4, S5, S7, S9
-78V	S1, S2, S7, S8, S9, S12

-104V	S1, S2, S7, S8, S10, S12
-130V	S1, S3, S8, S7, S12
-156V	S3, S4, S7, S8, S10, S12
-182V	S3, S4, S7, S8, S9, S12
-208V	S1, S2, S7, S8, S9, S11
-234V	S1, S2, S7, S8, S10, S11
-260V	S1, S3, S7, S8, S11
-286V	S3, S4, S7, S8, S10, S11
-312V	S3, S4, S7, S8, S9, S11

IV. PROPOSED SYSTEM OF 65 & 85 LEVEL ASYMMETRICAL CMLI

In this proposed system 65 & 85 level Asymmetrical Multi-cell CMLI is obtained. By this proposed system the THD value of 85 level Asymmetrical Multi-cell CMLI is reduced compared to the 65 level Asymmetrical Multi-cell CMLI.

By using other topologies, as the levels were increased simultaneously number of switches were also increased which may increase the switching losses that decreases the efficiency and life span is also decreases. Hence the main reason for using this topology is to improve the fundamental component and also to decrease the THD value and to get the staircase wave form. The 85level asymmetric multi-cell CMLI is as shown in Fig.6.

In this 65 level asymmetric multi-cell CMLI system have the input supply to the system is 10V, 10V, 50V, 50V, 100V, 100V. There are a total of 320 volts. There are total of three bridge circuits, each bridge has two inputs and the first bridge circuit consists of inputs as 10V and 10V, whereas second bridge circuit of 50V and 50V and third bridge circuit of 100V and 100V respectively.

In this 85 level asymmetric multi-cell CMLI system system have the input supply to the system is 7.76V, 7.76V, 38.80V, 38.80V, 116.4V, 116.4V. There are a total of 325.25 volts. There are total of three bridge circuits, each bridge has two inputs and the first bridge circuit consists of inputs as 7.76V and 7.76V, whereas second bridge circuit of 38.80V and 38.80V and third bridge circuit of 116.4V and 116.4V respectively.

Table II: Switching Table for Proposed System of 85 Level

Voltage	Switches
0V	S1,S3,S5,S7,S9,S11
7.76V	S1,S2,S5,S7,S9,S11,S14
15.52V	S1,S2,S5,S7,S9,S11,S13
23.28V	S3,S4,S5,S6,S9,S10,S13,S16
31.02V	S3,S4,S5,S6,S9,S11,S14,S16
38.80V	S1,S3,S5,S6,S9,S11,S16
46.56V	S1,S2,S5,S6,S9,S11,S14,S16
54.32V	S1,S2,S4,S6,S9,S11,S13,S16
62.08V	S3,S4,S5,S6,S9,S11,S13,S15
69.84V	S3,S4,S5,S6,S9,S11,S14,S15
77.6V	S1,S3,S5,S6,S9,S11,S15
85.36V	S1,S2,S5,S6,S9,S11,S14,S15
93.12V	S1,S2,S5,S6,S9,S11,S13,S15
100.88V	S3,S4,S5,S7,S9,S10,S13,S18
108.64V	S3,S4,S5,S7,S9,S10,S14,S18
116.4V	S1,S3,S5,S7,S9,S10,S12,S18
124.16V	S1,S2,S5,S7,S9,S10,S15,S18
131.92V	S1,S2,S5,S7,S9,S10,S13,S18
139.68V	S3,S4,S5,S6,S9,S10,S13,S16,S18
147.44V	S3,S4,S5,S6,S9,S10,S14,S16,S18
155.2V	S1,S3,S5,S6,S9,S10,S16,S18
162.96V	S1,S2,S5,S6,S9,S10,S14,S16,S18
170.72V	S1,S2,S5,S6,S9,S10,S13,S16,S18
178.48V	S3,S4,S5,S6,S9,S10,S13,S15,S18
186.24V	S3,S4,S5,S6,S9,S10,S14,S15,S18
194V	S1,S3,S5,S6,S9,S10,S15,S18
201.76V	S1,S2,S5,S6,S9,S10,S14,S15,S18
209.52V	S1,S2,S5,S6,S9,S10,S12,S14,S18
217.28V	S3,S4,S5,S7,S9,S10,S13,S17
225.04V	S3,S4,S5,S7,S9,S10,S14,S17
232.8V	S1,S3,S5,S7,S9,S10,S17
240.56V	S1,S2,S5,S7,S9,S10,S14,S17
248.32V	S1,S2,S5,S7,S9,S10,S13,S17
256.08V	S3,S4,S5,S6,S9,S10,S13,S16,S17
263.84V	S3,S4,S5,S6,S9,S10,S14,S16,S17
271.6V	S1,S3,S5,S6,S9,S10,S16,S17
279.96V	S1,S2,S5,S6,S9,S10,S14,S16,S17
287.12V	S1,S2,S5,S6,S9,S10,S13,S15,S17
294.88V	S3,S4,S5,S6,S9,S10,S13,S15,S17
302.64V	S3,S4,S5,S6,S9,S10,S14,S15,S17
310.4V	S1,S3,S5,S6,S9,S10,S15,S17
318.16V	S1,S2,S5,S6,S9,S10,S14,S15,S17
325.92V	S1,S2,S5,S6,S9,S10,S13,S15,S17

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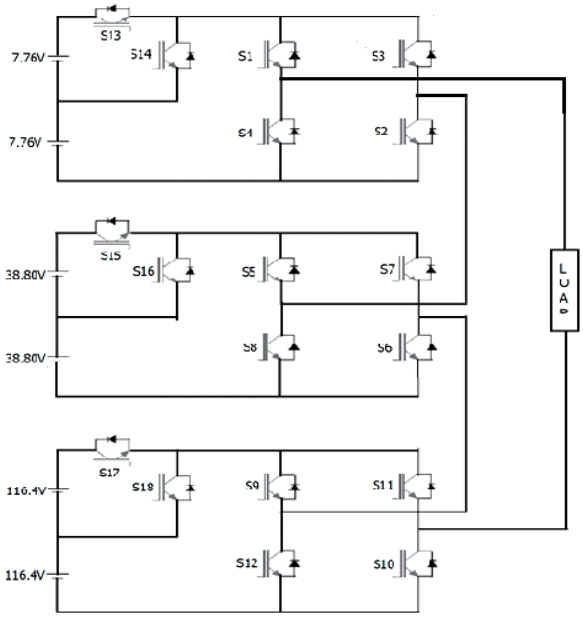

Fig. 6 Newly proposed 85 level Asymmetric multi-cell CMLI

The Fig.6 Shows Proposed 85 level asymmetric multi-cell CMLI having 18 switches and 6 DC sources but compared to Cascaded H-bridge MLI having 168 switches and 42 DC sources.

The proposed system is operated in 85 modes and these are controlled by changing the switching periods of the switching devices. The table showing the intervals of the switching at different levels of voltages is shown in table II. The different modes of operation are represented as following the table II determines which switches on and off in each level. For example, to get 0V as the output the switches like S1, S3, S5, S7, S9, S11 are triggered. Like that to get the 43th mode 325V as the output, the switches are S1, S2, S5, S6, S9, S10, S13, S15, S17 are triggered. Hence the current path will be written as 116.4V → -116.4V → S17 → S9 → S6 → -38.80V → 38.80V → S15 → S5 → S2 → -7.76V → - 7.76V → S13 → S1 → LOAD → S10 → 116.4V then the output will be V0= 325.95V. The THD of the proposed multi-cell CMLI is very low because the output can get 85 levels in its staircase waveform. To get the THD value are measured.

VI. SIMULATION RESULTS

I. Proposed system of Asymmetrical 65 & 85 level multi-cell CMLI

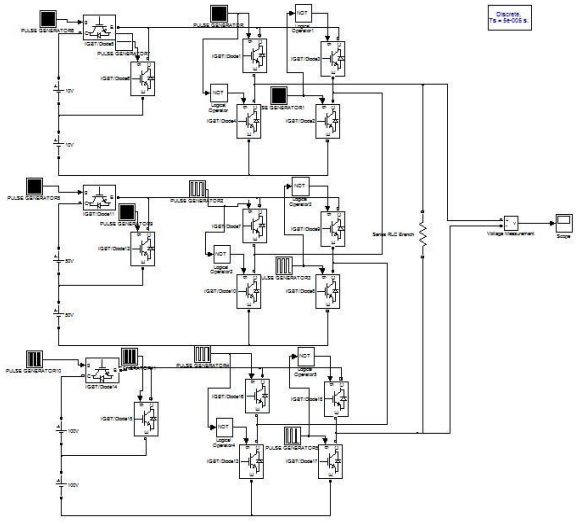

Fig. 7 Proposed system of Asymmetric 65 & 85 level multi-cell CMLI

The above Figure 7 shows proposed system of 65 & 85 level asymmetric multi-cell CMLI.

II. Proposed system of Asymmetrical 65 level output voltage of proposed asymmetric multi-cell CMLI

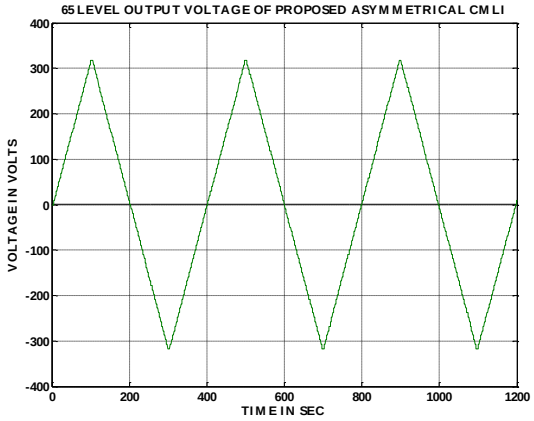

Fig. 8 Sixty five level output voltage of 65level newly proposed asymmetrical mutli-cell CMLI

The above Figure 8 shows Sixty five level output voltage produced from 65level proposed asymmetrical multi-cell CMLI

III. FFT analysis of Proposed system of 65 level asymmetric multi-cell CMLI

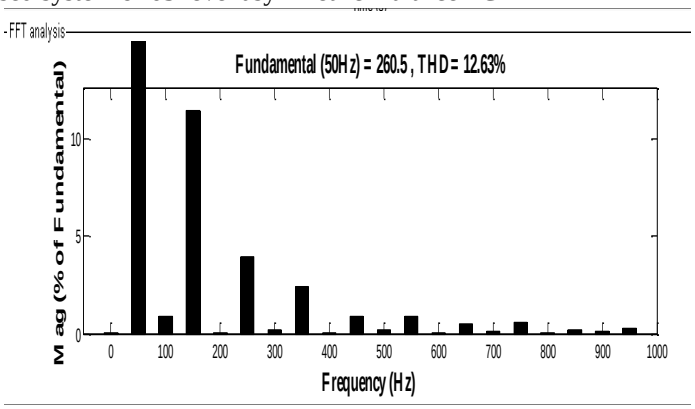

Fig. 9 FFT analysis of proposed 65level proposed asymmetrical CMLI

The above Fig.9 shows proposed system of 65 level asymmetric multi-cell CMLI to get THD value 12.63% and Fundamental component voltage is 260.5Volts

IV. Proposed system of Asymmetrical 85 level output voltage of proposed asymmetric multi-cell CMLI

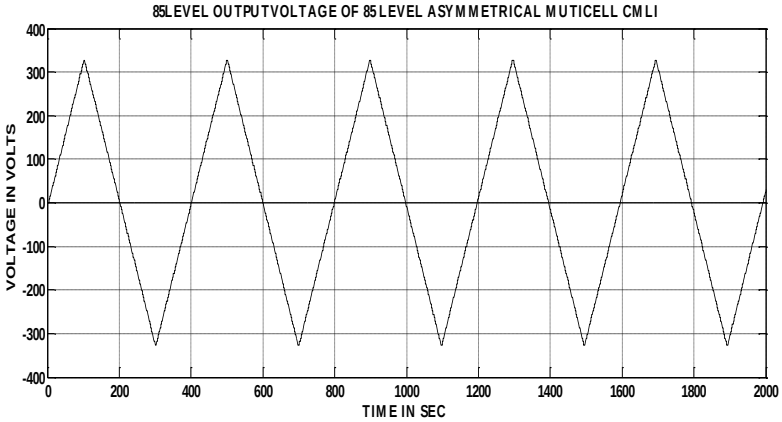

Fig. 10 Eighty five level output voltage of 85level proposed asymmetrical mutli-cell CMLI

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The above Fig.10 shows eighty five level output voltage produced from 85level proposed asymmetrical multi-cell CMLI

V. FFT analysis of Proposed system of 85 level asymmetric multi-cell CMLI

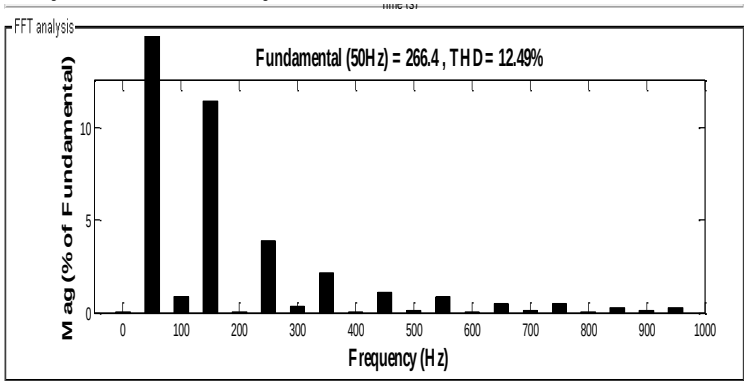

Fig. 11 FFT analysis of proposed 85level proposed asymmetrical CMLI

In proposed system of 85 level asymmetric multi-cell CMLI to get THD value 12.49% and Fundamental component voltage is 266.4Volts

VI. Newly Proposed system of Asymmetrical 85 level multi-cell CMLI with grid Connected system

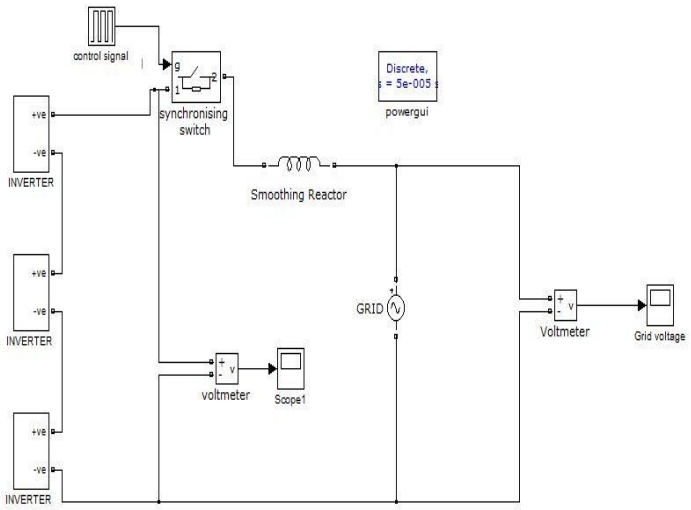

Fig. 12 Newly Proposed system of Asymmetrical 85 level multi-cell CMLI with grid Connected system

The above Fig.12 shows grid connected system of asymmetrical 85 level CMLI with distributed energy sources like PV cells.

VII. Distributed Renewable energy source of PV Cell Designing

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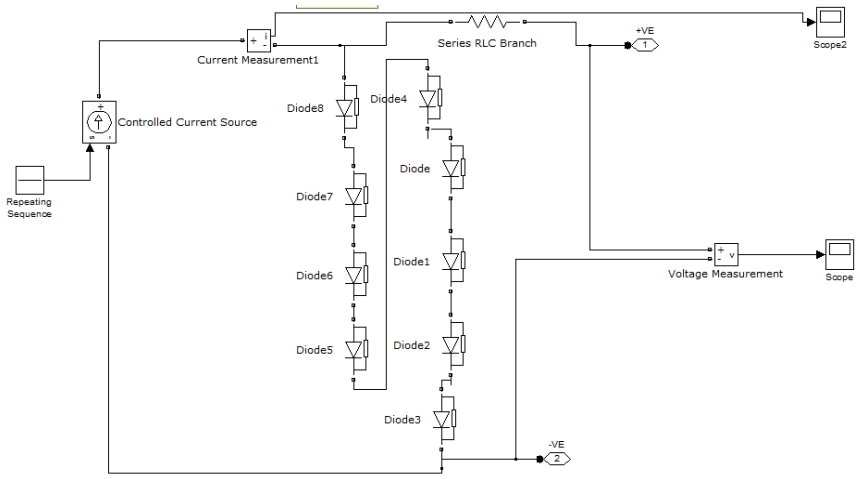

Fig. 13 PV cell designing of DRES of the input of converter 85 level asymmetrical multi-cell CMLI to grid

The above Fig.13 shows PV Cell designing of DRES of the input of eighty five level output voltage produced from 85 level proposed asymmetrical multi-cell CMLI.

VIII. Proposed system of Asymmetrical 85 level multi-cell CMLI with grid Connected system of grid voltage

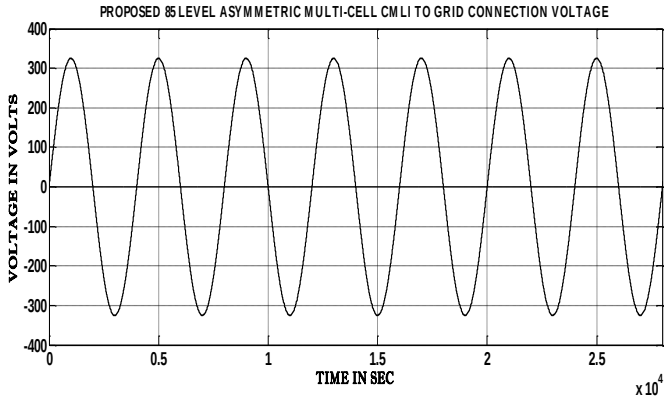

Fig. 14 Proposed system of Asymmetrical 85 level multi-cell CMLI with grid Connected system of grid voltage

The above Figure 14 shows grid voltage of proposed system of Asymmetrical 85 level multi-cell CMLI with grid connection.

Table III: Conventional Cascaded H-Bridge Configuration

Number of Levels	Required Number of Switches	Number of DC Sources
65 Level	128	32
85 Level	168	42

Table IV: Proposed Asymmetrical Multicell CMLI

Number of levels	Required number of switches	Number of DC sources
65 Level	18	6
85 Level	18	6

Table V: THD Comparison 65 & 85 Level Proposed System

Type of system	Required number of switches	Fundamental voltage In volts	THD (%)
Proposed system	65 LEVEL	260.5	12.63
Proposed system	85 LEVEL	266.4	12.49

In this paper Conventional CHB configuration of 7, 25, 65, 85 levels produce by using number of switches and number of DC sources in the table III. The same number of levels produces by using number of switches and number of DC sources in the table IV. The fundamental voltage is 266.4Volts and THD values is 12.49% in the proposed 85level asymmetrical multi-cell MLI best one compared to remaining in table V.

VI. CONCLUSION

Finally, Paper work is conceded out on, proposed system of 65 level and 85 level asymmetric multi-cell CMLI and were presented. The THD value attained by the proposed system of 65 level obtained THD value is 12.63% and also proposed system of 85 level obtained THD value is 12.49%. The distributed renewable energy sources are PV cells their input of proposed system of 85 level asymmetric multi-cell CMLI and also connected to grid.

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